AMENDMENTS TO THE CLAIMS:

Please amend claim 1 as follows:

1. (Currently Amended) A semiconductor memory device, comprising:

a memory cell array;

a decoder unit selecting a word line of the memory cell array;

a first dummy cell array connected to a first dummy bit line and disposed with the memory cell array at a first location away from the decoder unit along the word line;

a second dummy cell array connected to a second dummy bit ~~lines~~ line and disposed with the memory cell array at a second location away from the decoder unit along the word line, the second location being farther from the decoder unit than the first location;

a timing control unit determining timing of activation and deactivation of an internal control signal, wherein the timing control unit determines the timing of activation of the internal control signal based on a first signal passing the first dummy bit line through a corresponding dummy cell of the first dummy cell array, and determines the timing of deactivation of the internal control signal based on a second signal passing the second dummy bit line through a corresponding dummy cell of the second dummy cell array.

2. (Original) The semiconductor memory device of claim 1 wherein the first dummy cell array is disposed at a location nearest to the decoder unit, and the second dummy cell array is disposed at a location farthest from the decoder unit.

3. (Original) The semiconductor memory device of claim 2 wherein the timing control unit is provided to determine activation timing of a data latch signal, inputted to a

corresponding output latch portion of an I/O latch circuit, based on an output signal of a corresponding dummy cell of the first dummy cell array.

4. (Original) The semiconductor memory device of claim 2 wherein the timing control unit is provided to determine deactivation timing of a data latch signal, inputted to a corresponding output latch portion of an I/O latch circuit, based on an output signal of a corresponding dummy cell of the second dummy cell array.

5. (Original) The semiconductor memory device of claim 1 wherein the semiconductor memory device is an SRAM having no sense amplifier.

6. (Original) The semiconductor memory device of claim 1 wherein the first dummy cell array is disposed at a location nearest to the decoder unit, and the second dummy cell array is disposed nearly at a central location of the memory cell array.

7. (Original) The semiconductor memory device of claim 6 wherein the timing control unit is provided to determine activation timing of a data latch signal, inputted to a corresponding output latch portion of an I/O latch circuit, based on an output signal of a corresponding dummy cell of the first dummy cell array.

8. (Original) The semiconductor memory device of claim 6 wherein the timing control unit is provided to determine deactivation timing of a data latch signal, inputted to a corresponding output latch portion of an I/O latch circuit, based on an output signal of a corresponding dummy cell of the second dummy cell array.

9. (Original) The semiconductor memory device of claim 2 further comprising an odd number of inverters connected in series on the first dummy bit line to which the first dummy cell array is connected, and an even number of inverters connected in series on the second dummy bit line to which the second dummy cell array is connected.

10. (Original) The semiconductor memory device of claim 6 further comprising an odd number of inverters connected in series on the first dummy bit line to which the first dummy cell array is connected, and an even number of inverters connected in series on the second dummy bit line to which the second dummy cell array is connected.

11. (Original) The semiconductor memory device of claim 1 wherein the internal control signal is supplied to an I/O latch circuit, and the timing control unit determines activation and deactivation timing of a data latch signal which is inputted to the I/O latch circuit.

12. (Original) The semiconductor memory device of claim 1 wherein the internal control signal is supplied to a sense amplifier, and the timing control unit determines activation and deactivation timing of a sense amplifier activation signal which is inputted to the sense amplifier.